CLAIMS

1. A method for self-testing, allocating and repairing a Random Access Memory (RAM) using a spare column and spare rows, comprising:

performing first and second passes of self-test on the RAM memory;

in the first pass of self-test, determining a worst failing column of the RAM memory;

after completion of the first pass of self-test, allocating the spare column to replace the worst failing column;

in the second pass of self-test, determining unique failing row addresses in the memory;

after completion of the second pass of self-test, allocating the spare rows to replace the failing rows.

2. The method of claim 1, wherein after completion of the second pass of self-test, transporting the failing column and unique failing row addresses to e-fuse macros for permanent storage in the RAM memory.

3. The method of claim 1, wherein determining the worst failing column comprises testing one column at a time while counting the number of unique failing row addresses of the tested column by masking all columns except the tested column, such that only the un-masked tested column can produce an error in a data-out comparator.

4. The method of claim 3, wherein a decoder is used to mask all columns except the tested column.

5. The method of claim 4, wherein during the first pass of self-test a Built-In Self Test (BIST) generates a column address signal designating a particular column in memory to be selected and tested, which is input to said decoder to select the particular column to be tested, and during normal operation of the RAM a stored worst column address signal is decoded by decoder to implement the redundant data column in place of the worst tested column.

6. The method of claim 3, wherein a pass/fail signal from the data-out comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address.

7. The method of claim 3, wherein as each unique failing row address is stored, a counter is enabled to count the number of unique failing row addresses for the unmasked column, and at the end of testing of the unmasked column, if the error count value for the unmasked column exceeds a previously stored high error count value from previously tested columns, then the unmasked column is determined to be the worst column so far, and the error count value for the unmasked column is stored in an error count register, and a bit-address for the unmasked column is stored in a repair register.

8. The method of claim 7, wherein after completion of the first pass of self-test, the stored bit-address stored in the repair register is used to enable the spare column, prior to the second pass of the self-test, and a decoder is used to select steering multiplexers for implementing the spare column.

9. The method of claim 6, wherein during the second pass of self-test, the FAR stores unique failing row addresses, and at the end of the second pass of self-test, the FAR values are used to allocate and implement the spare rows.

10. The method of claim 1, wherein a Built-In Self Test (BIST) generates a column address signal designating a particular column in memory to be selected and tested, which is input to a first register which, which during BIST column testing, outputs the column address signal through a multiplexer to a decoder to select the particular column to be tested, the first register also outputs the worst tested column address signal to a second repair register, and during normal operation of the RAM the second repair register outputs the stored worst column address through the multiplexer to said decoder to implement the redundant data column in place of the worst tested column.

11. The method of claim 1, wherein during the first pass of self-test, all columns except a selected tested column are masked or deselected such that only the un-masked selected column can produce an error in a data-out comparator, and a pass/fail signal from the data-out

comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address, and a counter is enabled to count the number of unique failing row addresses for the unmasked column.

12. The method of claim 11, wherein at the end of testing of the unmasked column, if the count value for the unmasked column exceeds a previously stored worst count value from previously tested columns, then the unmasked column is determined to be the worst column so far, the count value for the unmasked column is stored in an error count register, and a bit-address for the unmasked data column is stored in a repair register.

13. The method of claim 12, wherein after testing of each unmasked column, the FAR and failing row counter are cleared before testing the next column, and the stored count value is subsequently compared to a count value for a next column after testing is completed on the next column, and at the completion of testing of all columns, the bit-address of worst column is stored and saved.

14. The method of claim 1, wherein in wide RAMs, the RAM is divided into sections of adjacent columns, with each section having its own redundant column to replace a worst failing column in that section, and each section is tested in parallel with other sections of columns.

15. The method of claim 1, wherein when the number of unique failing row addresses in two columns exceeds the number of redundant rows in the RAM, the RAM is designated as unrepairable.

16. The method of claim 1, performed on an embedded RAM within a microprocessor or logic chip.